ISSN:0975-9646

Deepali Sharma et al, / (IJCSIT) International Journal of Computer Science and Information Technologies, Vol. 2 (4) , 2011, 1625-1632

Design and VLSI Implementation of DDR SDRAM Controller for High Speed Applications

Deepali Sharma[#] Shruti bhargava [#] Mahendra Vucha[*]

[#] Dept. of ECE, TIT, Bhopal, India.
*Research Fellow, MANIT, Bhopal & Asst. Professor, GGITM, Bhopal, India.

Abstract: ***Synchronous DRAM (SDRAM) has become a mainstream memory of choice in design due to its speed, burst access and pipeline features. For high-end applications using processors, the interface to the SDRAM is supported by the processor's built-in peripheral module. However, for other applications, the system designer must design a controller to provide proper commands for SDRAM initialization, read/write accesses and memory refresh. DDR SDRAM uses double data rate architecture to achieve high-speed data transfers. DDR SDRAM (referred to as DDR) transfers data on both the rising and falling edge of the clock. This DDR controller is typically implemented in a system between the DDR and the Processor. In this paper, the implementation has been done in VHDL by using Modelsim 6.4b and Xilinx ISE 9.2i and then stated the conclusion that it works at 150.2 clock frequency.***

Keywords: Synchronous DRAM, Column Access Strobe, Row Access Strobe, Field Programmable Gate Arrays.

I. INTRODUCTION

With Microprocessors getting faster every year, memory architectures must also improve to enhance overall system performance. The Next Generation of SDRAM is DDR, or Double Data Rate. Like SDRAM, DDR is Synchronous with the System Clock. Although similar, in that both are Synchronous, the big difference between DDR and SDRAM is that DDR reads data on both the Rising and Falling edges of the clock signal, while SDRAM only carries information on the rising edge of a signal. This improvement allows the DDR module to transfer data twice as fast as SDRAM. As an example, instead of a data rate of 133MHz, DDR memory transfers data at 266MHz.DDR modules, like their SDRAM predecessors, arrive in there. Although motherboards designed to implement DDR are similar to those that use SDRAM, they are not backward compatible with motherboards that support SDRAM. You cannot use DDR in earlier SDRAM based motherboards, nor can you use SDRAM on motherboards that are designed for DDR.

A. Random Access Memory

Random access memory (RAM) is the best known form of computer memory. RAM is considered "random access" because you can access any memory cell directly if you know the row and column that intersect at that cell. RAM data, on the other hand, can be accessed in any order. All the data, whopalich the PC uses and works with during operation, are stored here. Data are stored on drives, typically the hard drive. However, for the CPU to work with those data, they must be read into the working memory storage (RAM).

B. Types of Random Access Memory

i. Static Random Access Memory

Static Random Access Memory uses a completely different technology. In static RAM, a form of flip-flop holds each bit of memory. A flip-flop for a memory cell takes four or six transistors along with some wiring, but never has to be refreshed. This makes static RAM significantly faster than dynamic RAM. However, because it has more parts, a static memory cell takes up a lot more space on a chip than a dynamic memory cell. Therefore, you get less memory per chip.

Static Random Access Memory uses multiple transistors, typically four to six, for each memory cell but doesn't have a capacitor in each cell. It is used primarily for cache. So static RAM is fast and expensive, and dynamic RAM is less expensive and slower. So, static RAM is used to create the CPU's speed-sensitive cache, while dynamic RAM forms the larger system RAM space.

ii. Dynamic Random Access Memory

Dynamic Random Access Memory has memory cells with a paired transistor and capacitor requiring constant refreshing. DRAM works by sending a charge through the appropriate column (CAS) to activate the transistor at each bit in the column. When writing the row lines contain the state the capacitor should take on. When reading the sense-amplifier determines the level of charge in the capacitor. If it is more than 50 percent, it reads it as a 1 otherwise it reads it as a 0.

A memory chip rating of 70ns means that it takes 70 nanoseconds to completely read and recharge each cell. One of the most common types of computer memory (RAM). It can only hold data for a short period of time and must be refreshed periodically. DRAMs are measured by storage capability and access time. Storage is rated in megabytes (8 MB, 16 MB, etc). Access time is rated in nanoseconds (60ns, 70ns, 80ns, etc) and represents the amount of time to save or return information. With a 60ns DRAM, it would require 60 billionths of a second to save or return information. The lower the speed, the faster the memory operates. DRAM chips require two CPU wait states for each execution. Can only execute either a read or write operation at one time. The capacitor in a dynamic RAM memory cell is like a leaky bucket. It needs to be refreshed periodically or it will discharge to 0. This refresh operation is where dynamic RAM gets its name.

Memory is made up of bits arranged in a two-dimensional grid. In which memory cells are etched onto a silicon wafer in an array of columns (bit lines) and rows (word lines). The intersection of a bit line and word line constitutes the address of the memory cell. Memory cells alone would be worthless without some way to get information in and out of them. So the memory cells have a whole support infrastructure of other specialized circuits.

Identifying each row and column (row address select and column address select) Keeping track of the refresh sequence (counter) Reading and restoring the signal from a cell (sense amplifier) Telling a cell whether it should take a charge or not (write enable) Other functions of the memory controller include a series of tasks that include identifying the type, speed and amount of memory and checking for errors. The traditional RAM type is DRAM (dynamic RAM). The other type is SRAM (static RAM). SRAM continues to remember its content, while DRAM must be refreshed every few milli seconds.

iii. Double Data Rate Synchronous Dynamic Random Access Memory

Double Data Rate Synchronous Dynamic Random Access Memory is the original form of DDR SDRAM. It is just like SDRAM except that is has higher bandwidth, meaning greater speed. Maximum transfer rate to L2 cache is approximately 1,064 MBps (for DDR SDRAM 133 MHZ).

DDR RAM is clock doubled version of SDRAM, which is replacing SDRAM during 2001-2002. Allows transactions on both the rising and falling edges of the clock cycle. It has a bus clock speed of 100MHz and will yield an effective data transfer rate of 200MHz. DDR come in PC 1600, PC 2100, PC 2700 and PC 3200 DIMMs. A PC 1600 DIMM is made up of PC 200 DDR chips, while a PC 2100 DIMM is made up of PC 266 chips. Go for PC2700 DDR. It is about the cost of PC2100 memory and will give you better performance. DDR memory comes in CAS 2 and CAS 2.5 ratings, with CAS 2 costing more and performing better.

II. HISTORICAL REVIEW

Back in the 80s, PCs were equipped with RAM in quantities of 64 KB, 256 KB, 512 KB and finally 1 MB. Think of a home computer like Commodore 64. It had 64 KB RAM, and it worked fine.

Around 1990, advanced operating systems, like Windows, appeared on the market, that started the RAM race. The PC needed more and more RAM. That worked fine with the 386 processor, which could address larger amount of RAM. The first Windows operated PCs could address 2 MB RAM, but 4 MB soon became the standard. The race has continued through the 90s, as RAM prices have dropped dramatically. Today no one is using less than 32 MB RAM in a PC. Many have much more. 128 MB is in no way too much for a "power user" with Windows 95/98, it is important with plenty of RAM.

SDRAM is widely used in computers, from the original SDRAM, further generations of DDR (or DDR1) and then DDR2 and DDR3 have entered the mass market, with DDR4 currently being designed and anticipated to be available in 2012.

Although the concept of synchronous DRAM has been known since at least the 1970s and was used with early Intel processors, it was only in 1993 that SDRAM began its path to universal acceptance in the electronics industry. In 1993, Samsung introduced its KM48SL2000 synchronous DRAM, and by 2000, SDRAM had replaced virtually all other types of DRAM in modern computers, because of its greater performance.

SDRAM latency is not inherently lower (faster) than asynchronous DRAM. Indeed, early SDRAM was somewhat slower than contemporaneous burst EDO DRAM due to the additional logic. The benefits of SDRAM's internal buffering come from its ability to interleave operations to multiple banks of memory, thereby increasing effective bandwidth.

Today, virtually all SDRAM is manufactured in compliance with standards established by JEDEC, an electronics industry association that adopts open standards to facilitate interoperability of electronic components. JEDEC formally adopted its first SDRAM standard in 1993 and subsequently adopted other SDRAM standards,

including those for DDR, DDR2 and DDR3 SDRAM.

SDRAM is also available in registered varieties, for systems that require greater scalability such as servers and workstations. As of 2007, 168-pin SDRAM DIMMs are not used in new PC systems, and 184-pin DDR memory has been mostly superseded. DDR2 SDRAM is the most common type used with new PCs, and DDR3 motherboards and memory are widely available, and less expensive than still-popular DDR2 products.

Today, the world's largest manufacturers of SDRAM include: Samsung Electronics, Micron Technology, and Hynix.

III. PROPOSED DDR SDRAM CONTROLLER

The functional block diagram of the DDR controller is shown in Figure 1. It consists of three modules, the main control module, the signal generation module and the data path module. The main control module has two state machines and a refresh counter, which generates proper istate and cstate outputs according to the system interface control signals. The signal generation module generates the address and command signals required for DDR based on istate and cstate. The data path module performs the data latching and dispatching of the data between the Processor and DDR.

The DDR SDRAM uses double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock- cycle data transfers at the I/O pins.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. As with standard SDR SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time. An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC standard for SSTL_2. All full-drive option outputs are SSTL_2, Class II compatible.

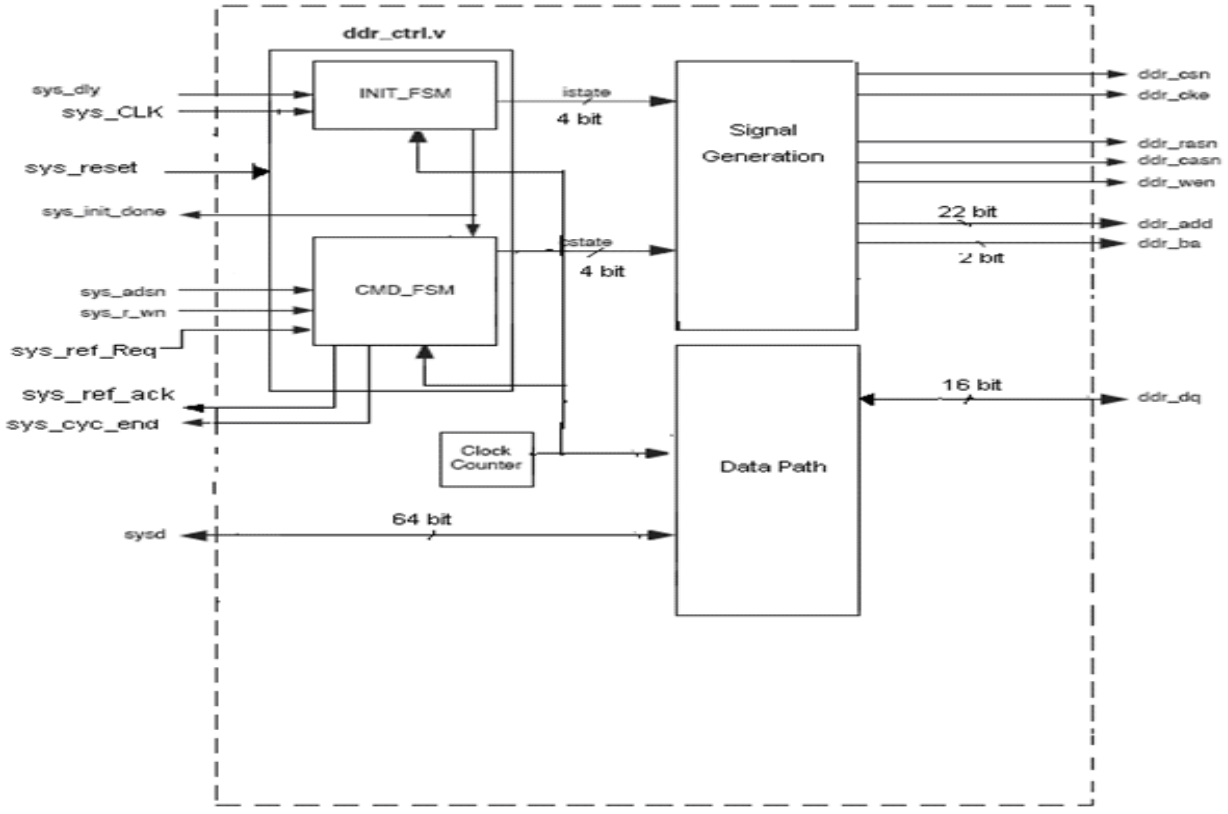

Fig. 1: Functional Block Diagram.

IV. DESIGN IMPLEMENTATION SCHEME

A. DDR SDRAM initial fsm

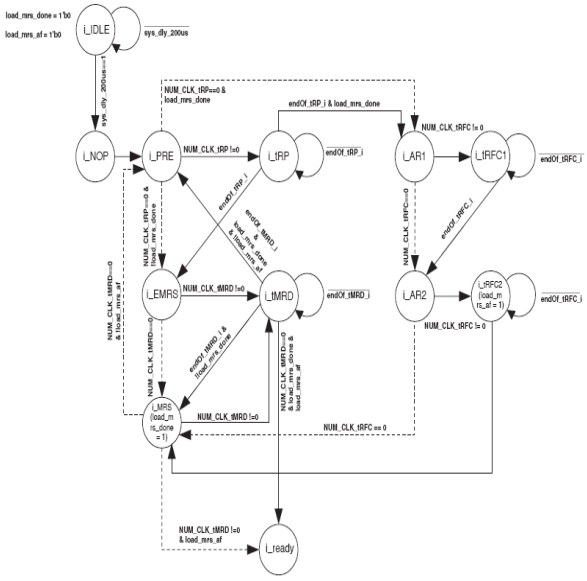

Fig.2 FSM diagram for initial state

i. Different states of Initial FSM:

Idle: When reset is applied the initial fsm is forced to IDLE state irrespective of which state it is actually in when system is in idle it remains idle without performing any operations.

*No Operation (NOP***):** The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Precharge (PRE): The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks as shown in Figure 3.3. The value on the BA0, BA1 inputs selects the bank, and the A10 input selects whether a single bank is precharged or whether all banks are precharged.

Auto Refresh (AR): AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS#-before-RAS# (CBR) refresh in DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued.

Load Mode Register (LMR): The mode registers are loaded via inputs A0–A*n*. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

Read/Write Cycle: The Figure 4.1 shows the state diagram of CMD_FSM which handles the read, write and refresh of the SDRAM. The CMD_FSM state machine is initialized to c_idle during reset. After reset, CMD_FSM stays in c_idle as long as sys_INIT_DONE is low which indicates the SDRAM initialization sequence is not yet completed.

Once the initialization is done, sys_ADSn and sys_REF_REQ will be sampled at the rising edge of every clock cycle. A logic high sampled on sys_REF_REQ will start a SDRAM refresh cycle. This is described in the following section. If logic low is sampled on both sys_REF_REQ and sys_ADSn, a system read cycle or system write cycle will begin. These system cycles are made up of a sequence of SDRAM commands.

B. DDR SDRAM command fsm:

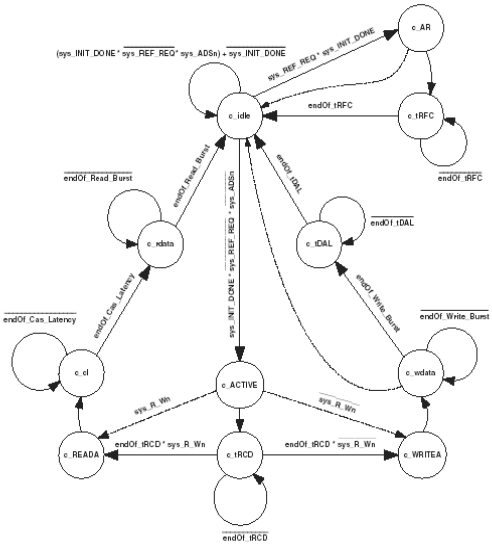

Fig. 3 FSM for Command state

i. Different states of Command FSM:

Refresh Cycle: DDR memory needs a periodic refresh to hold the data. This periodic refresh is done using AUTO REFRESH command. All banks must be idle before an AUTO REFRESH command is issued. In this design all banks will be in idle state, as every read/write operation uses auto pre charge.

Active (ACT): The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access, like a read or a write, as shown in Figure 4.2. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*n* selects the row.

Read: The READ command is used to initiate a burst read access to an active row, as shown in Figure 4.3. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where A*i* is the most significant column address bit for a given density and configuration) selects the starting column location.

Write: The WRITE command is used to initiate a burst write access to an active row as shown in Figure 4.4. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where A*i* is the most significant column address bit for a given density and configuration) selects the starting column location.

Refresh Cycle: Similar to the other DRAMs, memory refresh is required. A SDRAM refresh request is generated by activating sdr_REF_REQ signal of the controller. The sdr_REF_ACK signal will acknowledge the recognition of sdr_REF_REQ and will be active throughout the whole refresh cycle. The sdr_REF_REQ signal must be maintained until the sdr_REF_ACK goes active in order to be recognized as a refresh cycle. Note that no system read/write access cycles are allowed when sdr_REF_ACK is active. All system interface cycles will be ignored during this period. The sdr_REF_REQ signal assertion needs to be removed upon receipt of sdr_REF_ACK acknowledge,otherwise another refresh cycle will again be performed.

Upon receipt of sdr_REF_REQ assertion, the state machine CMD_FSM enters the c_AR state to issue an AUTO REFRESH command to the SDRAM. After tRFC time delay is satisfied, CMD_FSM returns to c_idle.

C. Signal generation

The figure 4 shows the signal generation module with inputs and outputs as shown in the figure. The signal generation module generates the address and command signals required for DDR based on istate and cstate and is shown in figure 5.

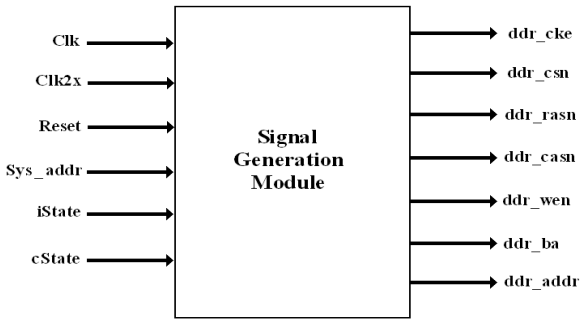

Fig. 4: Signal Generation Module.

Signal Generation flow chart:

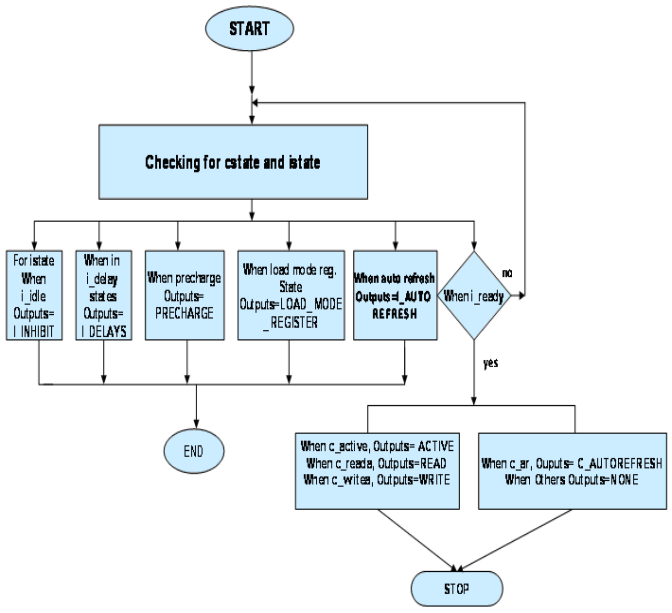

Fig. 5: Flow chart for Signal generator

D. Data path

The figure 6 shows the data path module with inputs and outputs as shown in the figure. The data flow design between the SDRAM and the system interface. The module in this reference design interfaces between the SDRAM with 16-bit bidirectional data bus and the bus master with 64-bit bidirectional data bus. The user should be able to modify this module to customize to fit his/her system bus requirements. The data path module performs the data latching and dispatching of the data between the processor and DDR.

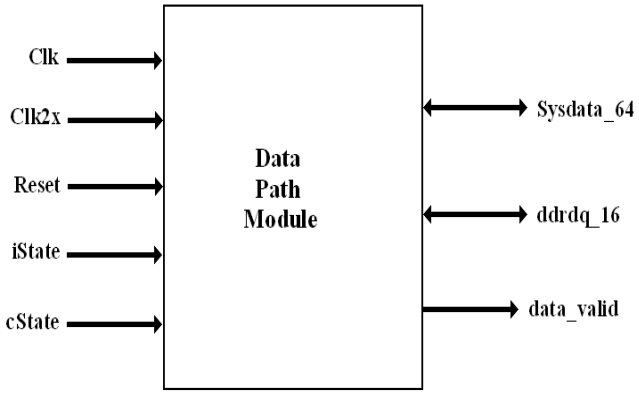

Fig. 6 : Data Path Module.

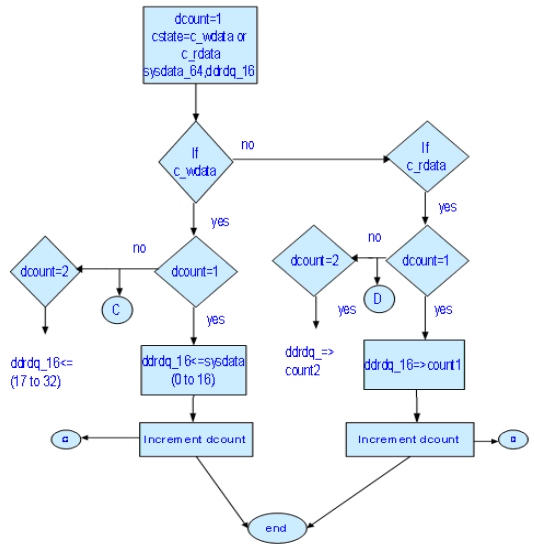

Fig. .7: Flow chart for Data path

V. RESULT & DISCUSSION

The Proposed design is simulated on Modelsim 6.4 and synthesized on Xilinx ISE 9.2 and then finally targeted to the Xilinx Spartan 3 FPGA device. The simulation and synthesis summary is shown bellow in fig. 8 , fig.9 and fig.10.

Table1. Synthesis Report

S.No	Component	Count
1	Speed	150.2MHz
2	Adders/ Subtractors	5
3	Counters	6
4	Registers	150

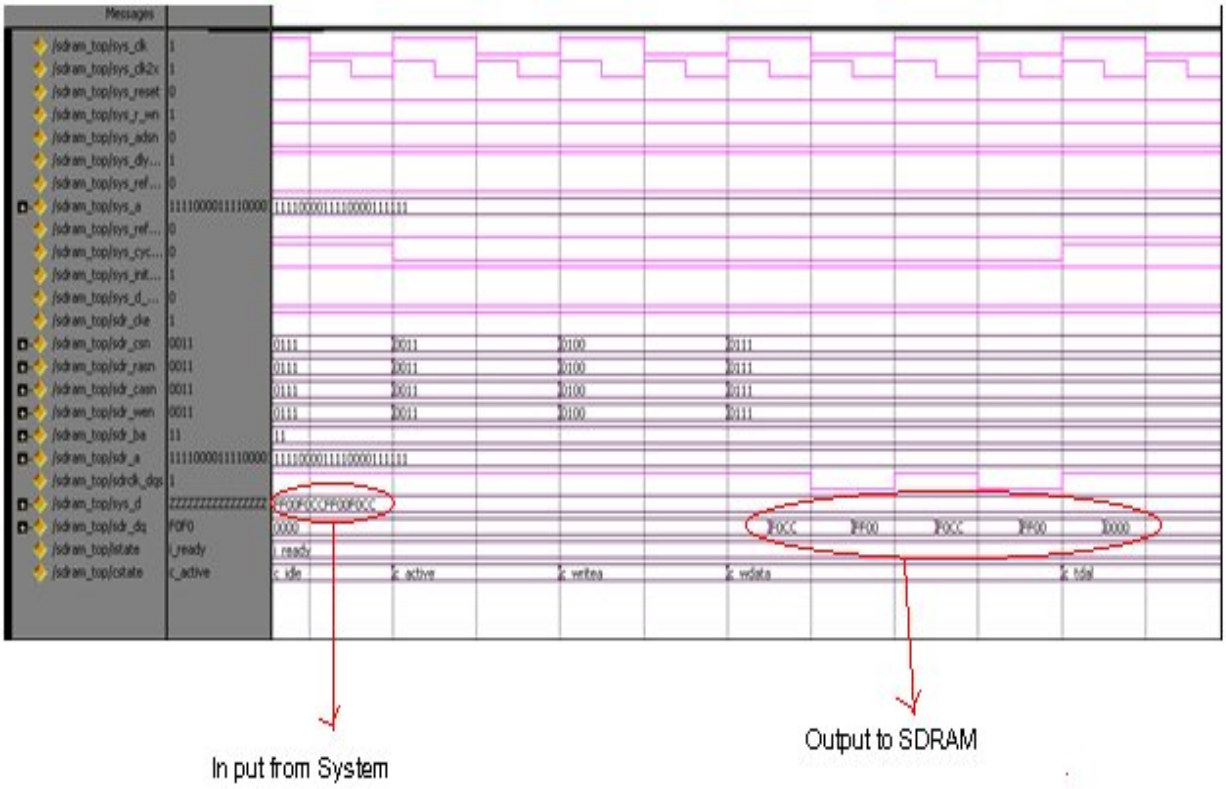

Fig.8: Simulation Waveforms of DDR controller

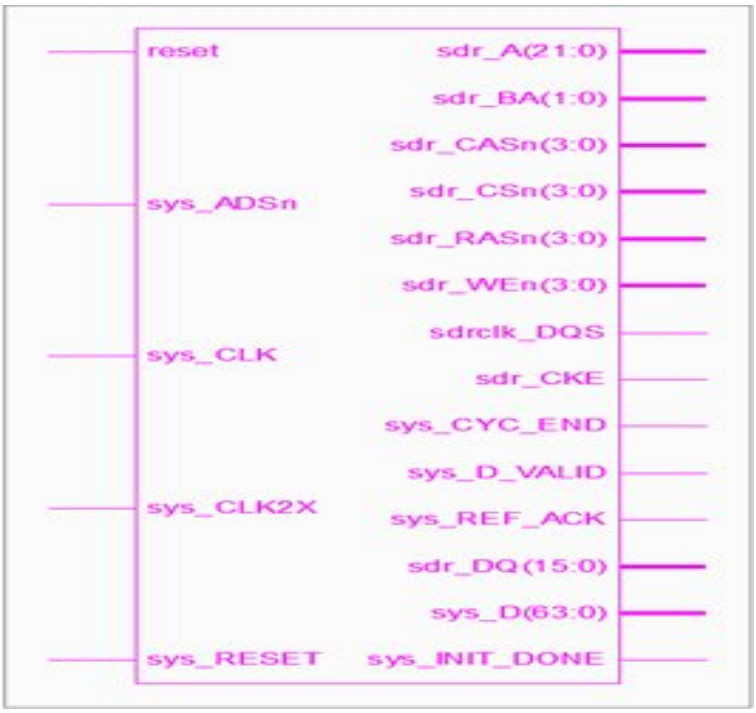

Fig .9 : RTL schematic of Top Module

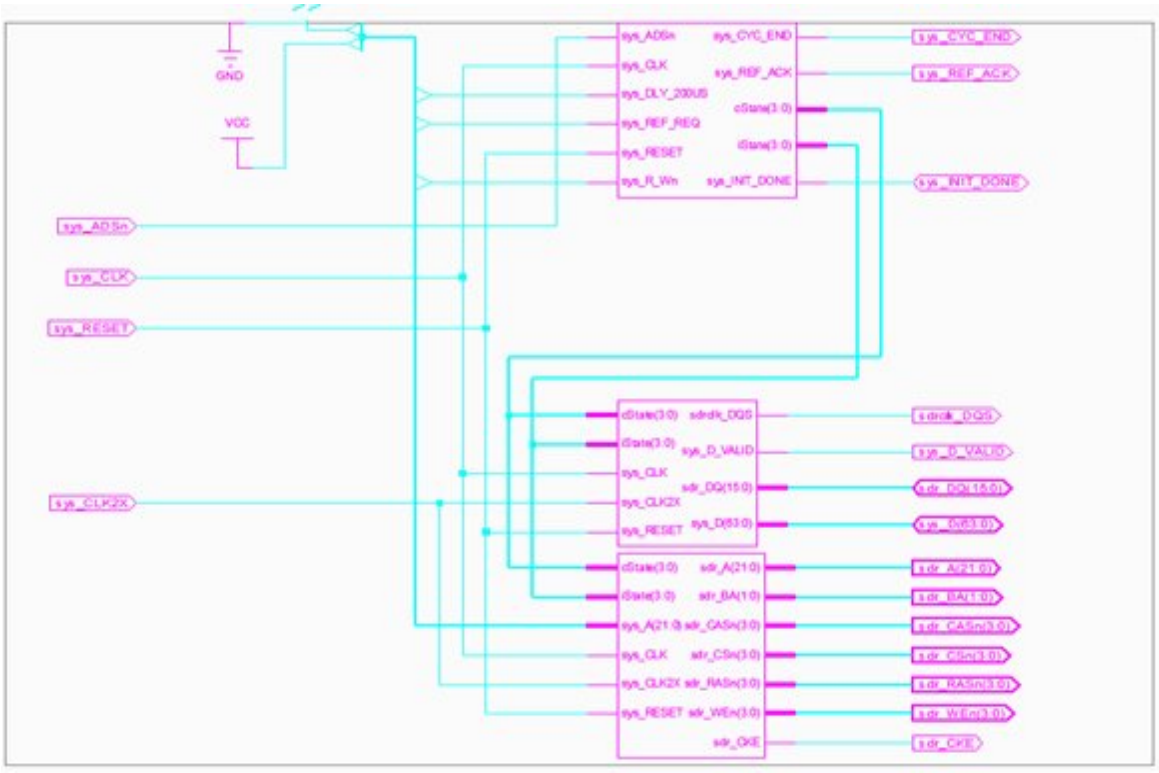

Fig.10: Internal hierarchy of Top level schematic

VI. CONCLUTION

The similarities between SDR and DDR SDRAM provide the DRAM manufacturer cost advantages and assure high production yields. These similarities also help the designer to better understand DDR and allow the most optimal design techniques from previous designs to be incorporated into the new DDR platforms. Although the addressing schemes, layout requirements, and device configurations are much the same for DDR, the performance gains are remarkable. For example, the power consumption for DDR is significantly less than for a comparable SDR device, yet peak transfer rates can exceed 2.1 GB/s for a standard x64 DDR.

Traditional single data rate (SDR) SDRAM architectures are performance-limited in their interfaces; therefore, DDR SDRAMs were introduced as an enhancement. While most of the addressing and command control interface is identical, the fundamental difference is in the data interface. Thus, this enables high-speed operation as the internal column accesses are half the frequency of the external data transfer rate.

DDR SDRAM is a volatile and complex memory device. When the power is removed, all contents and operating configurations are lost. Each time the memory is powered up, the device requires a defined procedure to initialize the internal state machines and to configure the various user-defined operating parameters. This project concentrates on the flow for the initialization sequence and the configurable device parameters.

REFERNCES

[1]. Burchardt, A., Hekstra-Nowacka, E., and Chauhan, A.,"A Real-time Streaming Memory Controller", Design, Automation and Test in Europe 2005 Proceedings, 2005, vol.3, pp. 20-25.
[2]. Heithecker, S. and Ernst, R., "Traffic Shaping for An FPGA Based SDRAM Controller with Complex QoSRequirements", Design Automation Conference *2005*,June 2005, pp. 575-578.
[3]. ANALOG DEVICES, AD9480 datasheet, Rev. *A*, 2004, 7.
[4]. ALTERA, DDR SDRAM Controller White Paper, Ver1.1, 2002, 8.
[5]. Guo Li, Zhang Ying, Li Ning, and Guo Yang, "TheFeature of DDR SDRAM and the Implementation of DDR SDRAM Controllers via VHDL", The Journal of China Universities of Posts and Telecommunications, 2002, vol.9,no. 1, pp. 61-65.
[6]. Digital Systems Design Using VHDL by Charles H. Roth, Jr
[7]. CMOS Designing by Kanzg
[8]. Basic Digital Design by Morris Mano
[9]. http://www.latticesemi.com/products/intellectualproperty/referencedesigns/ddrsdram controller.cfm
[10]. http://www.educypedia.be/computer/memorytypes.htm